PATENT ABSTRACTS OF JAPAN

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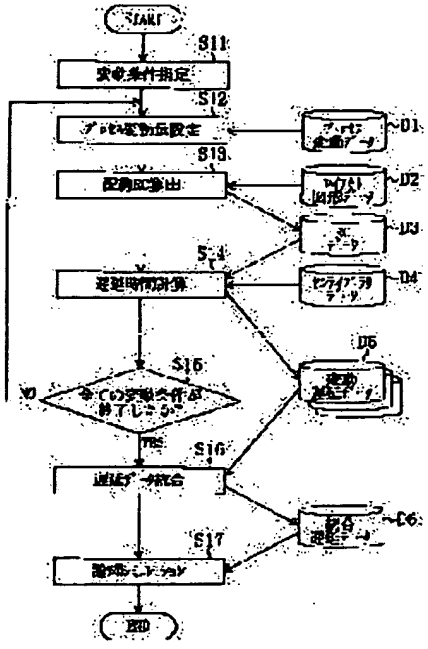
(54) TIMING VERIFYING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To efficiently perform timing verification while taking process variation into consideration.
SOLUTION: A stage for setting a process variation quantity to a process variation factor determined by a process for manufacturing a semiconductor integrated circuit, a stage for computing the resistance of wires and the line-to- line capacitance according to the process variation quantity and the layout figure of wires, and a stage for computing a 1st delay time of the wires and a 2nd delay time of a driving cell which drives the wires by using the resistance of the wires and the line-to-line capacitance are carried out at least twice while the process variation quantity is varied to computers at least two varying delay times consisting of the 1st delay time and 2nd delay time. According to at least the two varying delay times, a total delay time determining operation characteristics of the semiconductor integrated circuit is generated and then used to perform the logical simulation of the semiconductor integrated circuit.



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